

1       CLAIMS

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3     1. A circuit arrangement for deriving phase  
4       conjugation information from a main input signal  
5       of a given frequency comprising:

6       an input receiving a reference input signal;  
7       and

8       a phase locked loop (PLL) circuit comprising  
9       an oscillator having a main output signal, an  
10      input receiving a PLL input signal, an input  
11      receiving a feedback signal from the oscillator  
12      and a phase detecting means,

13      wherein the phase detection means detects any  
14      phase difference between the PLL input signal  
15      and the feedback signal and provides a phase  
16      control signal to the oscillator.

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18     2. A circuit as claimed in claim 1, wherein a first  
19       heterodyne mixer mixes the main input signal and  
20       the main output signal to provide the feedback  
21       signal and the PLL input signal is the reference  
22       input signal.

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24     3. A circuit as claimed in claim 2, wherein the  
25       feedback signal is the up-converted mixing  
26       product of the first heterodyne mixer.

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28     4. A circuit as claimed in claim 3, wherein the  
29       frequency of the reference input signal is  
30       scaled to match the frequency of the feedback  
31       signal.

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- 1       5. A circuit as claimed in any preceding claim,  
2            wherein the feedback signal is scaled.
- 3
- 4       6. A circuit as claimed in any preceding claim,  
5            wherein the phase detection means is a digital  
6            phase detector.
- 7
- 8       7. A circuit as claimed in any of claims 1 to 5,  
9            wherein the phase detection means also detects  
10          any phase difference between an input receiving  
11          the main output signal and an input receiving  
12          the reference signal thereby creating a further  
13          phase locked loop.
- 14
- 15      8. A circuit as claimed in claim 7, wherein the  
16          phase detection means comprises:
  - 17            a first phase detector which detects any phase  
18            difference between an input receiving the  
19            reference input signal and an input receiving  
20            the feedback signal;
  - 21            a second phase detector which detects any  
22            phase difference between an input receiving the  
23            reference input signal and an input receiving  
24            the main output signal;
  - 25            an integrator integrating the first phase  
26            detector output;
  - 27            an oscillator heterodyne mixer for mixing the  
28            integrator output and the second phase detector  
29            output;
  - 30            wherein the oscillator mixer output is the  
31            phase detection means output providing a control  
32            signal for the oscillator.

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2     9. A circuit as claimed in any of claims 1 to 5,  
3       wherein the phase detection means comprises:  
4            a first phase detection heterodyne mixer  
5            mixing an input receiving the reference input  
6            signal and an input receiving the feedback  
7            signal and having a first phase detection mixer  
8            output wherein the first mixer output is the  
9            down-converted mixing product of the first  
10          mixer;

11            a second phase detection heterodyne mixer  
12            mixing an input receiving the reference input  
13            signal and an input receiving the first phase  
14            detection mixer output and having a second phase  
15            detection mixer output wherein the second phase  
16            detection mixer output is the down-converted  
17            mixing product of the second phase detection  
18            mixer and the phase detection means output  
19            providing a control signal for the oscillator.

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21     10. A circuit as claimed in claim 1, wherein a  
22       feedback heterodyne mixer mixes an input  
23       receiving the main output signal and an input  
24       receiving the reference input signal, the  
25       feedback signal is the down-converted mixing  
26       product of the feedback heterodyne mixer and the  
27       PLL input signal is the main input signal, the  
28       feedback signal being proportional to the main  
29       input signal.

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31     11. A circuit as claimed in claim 10, wherein the  
32       main input signal is scaled by a first divider,

1       the main output signal is scaled by a second  
2       divider and the feedback signal scaled by a  
3       third divider, the first divider having a  
4       scaling value equal to the product of the second  
5       and third divider scaling values.

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7     12. A circuit as claimed in claim 1, wherein an input  
8       heterodyne mixer mixes the main input signal and  
9       the reference input signal, the PLL input signal  
10      is the down-converted mixing product of the  
11      input heterodyne mixer and the feedback signal  
12      is the main output signal, the main input signal  
13      and the main output signal having substantially  
14      equal frequencies.

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16     13. A circuit as claimed in claim 12, wherein a first  
17      divider scales the main input signal, a second  
18      divider scales the main output signal, the first  
19      divider having a scaling value equal to the  
20      second divider scaling value.

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22     14. A circuit as claimed in any preceding claim,  
23       wherein the oscillator is a voltage controlled  
24       oscillator (VCO).

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26     15. A method of deriving phase conjugation  
27       information from an input signal, the method  
28       comprising detecting phase difference in a phase  
29       locked loop (PLL) circuit between a feedback  
30       signal having a first frequency and a PLL input  
31       signal of a second frequency which is  
32       proportional to the first frequency.